IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A thermal interface material, comprising:

a polymer matrix;

fusible particles dispersed within the polymer matrix; and

non-fusible particles dispersed within the polymer matrix, wherein the fusible particles have a mean particle size that is greater than the maximum particle size of the non-fusible particles when fusible particles and non-fusible particles are blended together in the polymer matrix.

2. (Original) The thermal interface material of claim 1 wherein the polymer is a polymer solder hybrid.

3. (Original) The thermal interface material of claim 1 wherein the mean particle size of the fusible particles is less greater than or equal to about 60 microns.

4. (Original) The thermal interface material of claim 1 wherein the fusible particles have a size effective for contacting an upper and lower surface of two elements separated by the thermal interface material.

5. (Original) The thermal interface material of claim 1 wherein the fusible particles consist of indium and tin.

6. (Original) The thermal interface material of claim 1 wherein the fusible materials comprise In, Bi, Cu, Ag, Sn, Pb, Cd, Zn, Ga, Te, Hg, Tl, Sb, Se, Po, or mixtures of any two or more thereof or alloys thereof.

7. (Original) The thermal interface material of claim 1 wherein the polymer comprises one or more of siloxanes, olefins, and epoxies.

8. (Original) The thermal interface material of claim 1 wherein the polymer comprises a vinyl terminated polydimethylsiloxane, a crosslinker; a platinum catalyst; and an inhibitor.

9. (Original) An integrated circuit, comprising:

at least one silicon die;

the thermal interface material of claim 1; and

an integral heat spreader, wherein the thermal interface material is sandwiched between the silicon die and the integral heat spreader.

10. (Original) The integrated circuit of claim 9, wherein the fusible particles in the thermal interface material have a size effective for contacting both the integral heat spreader and the silicon die.

11. (Original) The integrated circuit of claim 9 further comprising a heat sink and a second thermal interface component, wherein the second thermal interface material component is sandwiched between the integral heat spreader and the heat sink.

12. (Original) The integrated circuit of claim 11 wherein the second thermal interface material component comprises the thermal interface material of claim 1.

13. (Currently Amended) The integrated circuit of claim 9 further comprising [[a]] a form factor.

14. (Previously Presented) The integrated circuit_ of claim 13 wherein the form factor is a ball grid array.

15. (Previously Presented) The integrated circuit of claim 13 wherein the form factor is a ball grid array with pinned interposers and wire bonding.

16. (Currently Amended) An electronic package, comprising:

a heat sink;

a thermal heat spreader; and

a thermal interface material, wherein the thermal interface material is sandwiched between the integral heat spreader and the heat sink further comprising fusible particles in the thermal interface material having a size effective for contacting both the heat sink and the integral heat spreader .

17. (Canceled)

18. (Original) An electronic assembly comprising the electronic package of claim 8.

19. (Original) An electronic assembly comprising the thermal interface material of claim 1.

20. (Original) An electronic assembly comprising the thermal interface material of claim 9.

21. - 23. (Canceled)

24. (Original) An electronic system comprising the integrated circuit of claim 9.

25. (Previously Presented) The integrated circuit of claim 13 wherein the form factor is a pin grid array.